RECEIVED
CENTRAL FAX CENTER

MAY 15 2007

DONALD R. ANTONELLI
MELVIN KRAUS
WILLIAM I. SOLOMON*
GREGORY E. MONTONE
RONALD J. SHORE
DONALD E. STOUT
ALAN E. SCHIAVELLI
PAUL J. SKWIERAWSKI*
ALFRED A. STADNICKI*
*ADMITTED OTHER THAN VA

LAW OFFICES
ANTONELLI, TERRY, STOUT & KRAUS, LLP
SUITE 1800
1300 NORTH SEVENTEENTH STREET
ARLINGTON, VIRGINIA 22209

TELEPHONE (703) 312-6600
FACSIMILE (703) 312-6666
gmontone@antonelli.com

OF COUNSEL
DAVID T. TERRY
HAROLD A. WILLIAMSON*
JESSICA H. BUI

PATENT AGENT
LARRY N. ANAGNOS

May 15, 2007

Honorable Commissioner for Patents
Alexandria, VA 22313

Central Fax - Facsimile No. 571-273-8300

Art Unit: 2185 Exr. M. ROJAS

Re: **K. KAKI et al - U.S. Appln. Ser. No. 10/784,995**
Attorney Docket No. 566.32253CC8

SUBMISSION of RE-SUBMITTED APPELLANT'S BRIEF

Sir:

Applicant hereby submits the attached paper entitled, "**SUBMISSION of RE-SUBMITTED APPELLANT'S BRIEF (19 pgs.)**" in the above-identified application.

CERTIFICATE OF TRANSMISSION:

I hereby certify that the attached paper entitled "SUBMISSION of RE-SUBMITTED APPELLANT'S BRIEF (19 pgs.)" is being formally filed in the USPTO via Facsimile No. 571-273-8300 on May 15, 2007.

David K. Snyder

566.32253CC8

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants:	K. KAKI et al.
Serial No.:	10/784,995
Filed:	February 25, 2004
Title:	SEMICONDUCTOR STORAGE APPARATUS IN WHICH DIFFERENT ERASE COMMANDS ARE SEQUENTIALLYSENT TO A PLURALTY OF NONVOLATILE SEMICONDUCTOR MEMORIES
Group:	2185
Examiner:	ROJAS, Midys
Confirmation No.:	9779

RE-SUBMITTED APPELLANT'S BRIEF

Mail Stop: Patent Appeals (Fee) **May 15, 2007**
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Sir:

In response to the Notification on Non-Compliant Appeal brief mailed May 4, 2007, the present Re-Submitted Appeal Brief is being submitted under 37 CFR §41.37, In connection with the appeal of the above-identified application. It is noted the previous heading "Summary of the Invention" has been changed to read "Summary of the Claimed Subject Matter" in this Re-Submitted Brief in response to the May 4, 2007 Notification . A Notice of Appeal was timely filed on October 12, 2006.

REAL PARTY IN INTEREST

The real party in interest is Renesas Technology Corp. of Japan.

RELATED APPEALS AND INTERFERENCES

None.

STATUS OF CLAIMS

Claims 1-17 are pending in this application. A copy of claims 1-17 which are on appeal appear in the appendix hereto. (Appendix A)

STATUS OF AMENDMENTS

The present Appeal Brief is being filed together with a Request for Reconsideration and Removal of Rejection, which requests removal of the prior art rejection to which this Appeal brief is directed. Accordingly, consideration of the Request for Reconsideration and Removal of Rejection prior to consideration of this Appeal Brief is requested.

The last Amendment filed in this application was filed on June 23, 2005, in response to the Office Action dated March 23, 2005. Following this, a Final Rejection was mailed on September 21, 2005. Applicants filed a Request for Reconsideration on January 30, 2006, which was answered by another Final Rejection mailed on March 6, 2006. Applicants responded to this second Final Rejection with another Request for Reconsideration on June 6, 2006, which was responded to by another Final Rejection mailed on July 12, 2006, citing new prior art utilized in a new rejection. No Amendment has been filed in response to the July 12, 2006 Final Office Action. Rather, a Request for Reconsideration was filed on October 12, 2006, which was answered by an Advisory Action of November 17, 2006.

SUMMARY OF CLAIMED SUBJECT MATTER

The present invention is directed to an improved arrangement for a semiconductor storage apparatus which facilitates more efficiently erasing data in a plurality of nonvolatile semiconductor memories.

Both of the independent claims 1 and 16, which are the only independent claims in this application, and which are on appeal, recite a semiconductor storage apparatus coupled to a system bus. Referring to Fig. 1, showing a first embodiment of the invention, for example, a semiconductor storage apparatus is illustrated connected to a system bus identified with the numeral 1. A plurality of nonvolatile semiconductor memories, such as the flash memories identified with the numeral 4 in Fig. 1, are provided to store sectors of data therein (noting that each sector of data is identified as including 512 bytes [e.g., see page 15, line 5 et seq.]). A control module, which can include the elements of the processor 2 and the address controller 31, in Fig. 1 is coupled with the system bus 1 and the nonvolatile semiconductor memories 4.

The present claims are particularly directed to the feature of an improved erase operation which can be achieved in the present invention. A discussion of the improved erase operation can be found, for example, beginning on page 16, line12 et seq. Fig. 4 also provides one example of a flow chart of such an improved erase operation, and discussion of Fig. 4 begins on page 17, line 10 et seq.

As specified in both of the independent claims 1 and 16, the control module sends a first erase command to one of the plurality of nonvolatile semiconductor memories 4 to initiate a first internal erase operation of data within that nonvolatile semiconductor memory. In conjunction with this, an important feature specified by

each of the independent claims 1 and 16 is that, after the first erase command has been sent, the control module:

> "sends a second erase command to another of said plurality of nonvolatile semiconductor memories, different from said one of said nonvolatile semiconductor memories to which said first erase command was sent, to initiate a second internal erase operation of data within said other of said plurality of nonvolatile semiconductor memories while said one of said plurality of non-volatile semiconductor memories is still performing said first internal erase operation responsive to said first erase command."

This is specifically discussed, for example, on page 16, line 20 et seq. of the Specification as follows:

> "Thus, an erase process within the flash memories 4 is started. Then, a latency of a predetermined time period is involved until the erase process within the flash memories 4 ends. Meanwhile, the flash memories 4 under the erase process cannot be accessed except for the status polling thereof. When the end of the internal erase process has been acknowledged by the status polling upon the lapse of the predetermined time period, the operation of erasing the next data from the designated one of the flash memories 4 is begun. During the predetermined time period, an erase command is written into another of the flash memories 4 different from the flash memory 4 which is under the erase process. Thus, the plurality of flash memories 4 are erased in parallel. Accordingly, the operation speed for erasing data with respect to the whole semiconductor disk pack is increased."

Accordingly, as can be seen from the above discussion, the independent claims 1 and 16 are each directed to the improved feature of providing an erase process for two separate nonvolatile semiconductor memories at the same time, to specifically offset the latency problem in erasing which exists in such nonvolatile semiconductor memories (as discussed beginning on page 16, line 12 et seq.).

The dependent claims define further features of the present invention. For example, dependent claim 2 defines the feature of a buffer memory, such as shown by the numeral 5 in Fig. 1, commonly coupled to the plurality of nonvolatile semiconductor memories (such as the flash memories 4 of Fig. 1) to hold the sectors

of data as write data to be written into each of the plurality of nonvolatile semiconductor memories. Dependent claim 2 further defines that the control module responds to a write request to carryout read operations of the first and second sectors of data as said write data from the buffer memory and carries out write operations of the sectors of data as data read out from the buffer memory into the plurality of nonvolatile semiconductor memories. In particular, dependent claim 2 defines an operation, in conjunction with the erase operation of its parent claim 1, in which a first write command from the command module is sent to one of the nonvolatile semiconductor memories and a second write command is sent to another one of the nonvolatile semiconductor memories, different from the nonvolatile semiconductor memory to which the first write command has been sent, while said one of said plurality of nonvolatile semiconductor memories is still performing a write operation responsive to said first write command. This is discussed, for example, on page 12, line 3 et seq. of the Specification. As such, dependent claim 2 represents a combination of both improved erase operations and improved write operations carried out by the semiconductor storage apparatus of the present invention.

Dependent claims 3, 4, 10 and 11 each define that the nonvolatile semiconductor memories can be comprised of flash memory semiconductor chips, as shown by the flash memories 4 of Fig. 1, for example. Dependent claims 6-9 and 12-15 define that the control module can include either a processor (such as identified by numeral 2 in Fig. 1) and/or an address controller (e.g., such as identified by numeral 31 in Fig. 1). Dependent claims 5, 10 and 11 each specify that the sectors are each in units of 512k bytes, which is the sector capacity of a standard disk, as discussed, for example, on page 15, line 5 et seq. Finally, dependent claim 17 defines that the control module carries out a status polling operation, as

discussed, for example, in the paragraph bridging pages 16 and 17 of the Specification.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1-17 stand rejected under 35 USC §103(a) as being unpatentable over USP 5,724,544 to Nishi in view of USP 5,664,145 to Apperley.

ARGUMENTS

As discussed above, each of the independent claims include the feature that after a first erase command is sent to one nonvolatile semiconductor memory, a second erase command is sent to another of the semiconductor memories to initiate a second internal erase operation of data within the nonvolatile semiconductor memory while the first erase operation in the first nonvolatile semiconductor memory is still being performed in response to the first erase command.

The July 12, 2006 Final Office Action recognizes in the third paragraph on page 3 that the primary reference to Nishi (USP 5,724,544) fails to teach "initiating the second erase command while the first erase operation is still being performed in the first non-volatile memory." In addition, in this third paragraph on page 3 of the Office Action, it is also apparently recognized that Apperley (USP 5,664,145) fails to disclose this limitation regarding initiating the second erase command while the first erase command is still being performed in a first non-volatile memory. Instead, the Office Action simply refers to the general teaching of Apperley with the statement that:

> "Apperley discloses running commands in parallel (col. 13, lines 24-29)."

Therefore, the Office Action goes on to state that this general teaching of Apperley regarding running commands in parallel would be sufficient to motivate one of ordinary skill in the art to modify the system of Nishi to perform erase operations in parallel in order to ensure minimum memory latency.

In response to this, applicants respectfully note that Apperley (USP 5,664,145) is not even directed to non-volatile semiconductor memories. Further, as noted above, Apperley does not provide any teachings with regard to timing for initiating internal erase operations of data for such non-volatile semiconductor memories to compensate for slow processing in such non-volatile memories. In short, the only actual motivation for making the substantial modifications to Nishi, which does use non-volatile memories, is the applicants' own teachings. MPEP 2143.01 clearly specifies that motivation to modify a reference "either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art." MPEP 2143.01 goes on to note that the mere fact t hat the references could be combined or modified is not sufficient to establish prima facie obviousness. MPEP 2143.01 also notes that the "fact that the claimed invention is within the capabilities of one of ordinary skill in the art is not sufficient by itself to establish prima facie obviousness."

With regard to the fundamental test set forth in MPEP 2143.01 that motivation must be found either explicitly or implicitly in the references themselves, this is clearly not the case in the present instance since the reference to Apperley, relied on for the modifications, teaches neither non-volatile semiconductor memories nor initiating a second erase command while a first erase operation is still being performed in a first non-volatile memory. Therefore, it is urged that the combination of Apperley and Nishi fails to meet the test required in MPEP 2143.01.

With regard to falling with common knowledge in the art, it is noted that MPEP 2144.03 states that such reliance should be rare and:

> "Official notice unsupported by documentary evidence should only be taken by the Examiner where the facts asserted to be well known, or to be common knowledge in the art are capable of instant and unquestionable demonstration as being well known."

It is urged that initiating second erase commands for a second non-volatile memory while the first erase operation is still being performed in a first non-volatile memory certainly is not "capable of instant and unquestionable demonstration as being well known." Therefore, it is respectfully submitted that the combination and modification proposed in the present rejection clearly fails to meet the requirements of either MPEP 2143.01 or 2144.03.

In the Advisory Action dated November 17, 2006, the Examiner argues that although Nishi does not teach two erase commands being processed in parallel, the Nishi reference does teach the initiation of two erase commands (apparently at completely separate times, with the second erase command being initiated only after the completion of the first erase command). As such, Nishi will obviously completely lack the advantage of the present invention, described on page 17, lines 7-9, of increasing the operating speed for erasing data for the whole semiconductor disk pack. However, the statements in the Advisory Action go on to state:

> "The Apperley reference is being used as support of the teaching that it as advantageous to perform commands in parallel for the purpose of minimizing latency. Apperley does not teach performing two erase commands in parallel, but simply teaches performing command processes in general in parallel (which includes the parallel processing of reads, writes, or erase commands). "

In particular, on page 3 of the Final Office Action, reference is made to the teachings of Apperley found in column 13, line 24-29. This portion of the Apperley reference simply states:

> "The command process (one of four subtasks of the command control task) processes the SCSI commands on the Device Command queues. There are four instances of the command process running in parallel, one for each of the four supported devices. Normally, each process handles commands addressed to its device. "

It is respectfully submitted that this very brief reference in Apperley to running commands in parallel clearly fails to meet the limitations found in both of the independent claims 1 and 16. Specifically, each of these claims defines that after a first erase command has been sent, a second erase command is sent to a different nonvolatile semiconductor memory to initiate the second internal erase operation. In addition to the fact that Apperley does not deal with resolving a latency problem in nonvolatile semiconductor memories, and does not deal with the parallel operation of erase commands, there is no teaching or suggestion for the order of the erase commands specified in the independent claims 1 and 16, specifically, that the second erase command is not generated until after the first erase command has been sent. This requirement for the second erase command to be sent after the first erase command has already been sent corresponds to the discussion in the Specification with regard to the step 45 shown in Fig. 4. Specifically, in accordance with the present claimed invention defined in independent claims 1 and 16, an operation is carried out by the control module to determine whether a "next erase area" exists, after an erase command has already been sent. There is absolutely no discussion found in Apperley, or Nishi, concerning any such ordered operation for the generation of a second erase command only after the first erase command has

been sent. Therefore, it is urged that this represents a further distinction over the combined teachings of Nishi and Apperley.

As discussed above, dependent claim 2 combines the features of a parallel write operation with the parallel erase operation. This serves to provide a semiconductor storage apparatus which has reduced latency both for a write operation and an erase operation. Again, it is urged that there is absolutely nothing in the brief reference to parallel command processes in Apperley which would at all suggest the claimed features of dependent claim 2 (combined with the features of claim 1, for reducing the latency of both the write operations and the erase operations in nonvolatile semiconductor memories.

Dependent claim 17 specifically defines that the control module:

> "Carries out a status polling operation in an order of said nonvolatile semiconductor memories to which said control module sent said erase commands, after said control module sent said erase commands to all of said nonvolatile semiconductor memories."

As discussed above, this polling operation of the control module, is discussed, for example, in the paragraph bridging pages 16 and 17 of the Specification. This polling operation is specifically in conjunction with the claim generation of the first and second erase commands set forth in the parent claim 16. In other words, the status polling operation defined in dependent claim 17 is taken in conjunction with the generation of the second erase command only after the first erase command has been generated, such that both the first and second erase operations are carried together. Inasmuch as the primary reference to Nishi clearly fails to teach or suggest the claimed features for the timing of the first and second internal erase operations defined by claim 16, as recognized in the Office Action, there is absolutely nothing with regard to the Apperley reference which would suggest the further features of

claim 17 concerning the use of the status polling operation in conjunction with the first and second erase command features of claim 16.

Dependent claims 5, 10 and 11 each define the feature that the sectors are in units of 512k bytes, which is the sector capacity of a standard disk. It is respectfully submitted that this specific feature, regarding the sector capacity, in conjunction with the features of the independent claim 1 and the dependent claim 2 (in the case of claims 5 and 11) as clearly not suggested by either of the cited references to Nishi and Apperley.

Finally, the dependent claims 3, 4, 6-9 and 12-15 define overall structural features of the control module and the nonvolatile semiconductor memories which, when considered in conjunction with the overall features of their respective parent claims, represent further distinctions over the cited prior art.

CONCLUSION

For the foregoing reasons, appellants request that the Examiner's rejections be reversed.

The Appeal Brief Fee was previously submitted on March 12, 2007.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to the Antonelli, Terry, Stout & Kraus, LLP

Deposit Account No. 01-2135 (Docket No. 566.32253CC8), and please credit any excess fees to such deposit account.

Respectfully submitted,
ANTONELLI, TERRY, STOUT & KRAUS, LLP

By _____
Gregory E. Montone
Reg. No. 28,141

GEM/dks

Enclosures: Appendix A (Claims)
Evidence Appendix
Related Proceedings Appendix

APPENDIX A

1. A semiconductor storage apparatus to be coupled with a system bus to receive a write request accompanied with first and second sectors of data, comprising;

a plurality of nonvolatile semiconductor memories which store said first and second sectors of data therein; and

a control module to be coupled with said system bus, and coupled with said plurality of nonvolatile semiconductor memories,

wherein said control module sends a first erase command to one of said plurality of nonvolatile semiconductor memories to initiate a first internal erase operation of data within said one of said plurality of nonvolatile semiconductor memories, and

whereln, after said first erase command has been sent, said control module sends a second erase command to another of said plurality of nonvolatile semiconductor memories, different from said one of said plurality of nonvolatile semiconductor memories to which said first erase command was sent to initiate a second internal erase operation of data within said other of said plurality of nonvolatile semiconductor memories while said one of said plurality of nonvolatile semiconductor memories is still performing said first internal erase operation responsive to said first erase command.

2. A semiconductor storage apparatus according to claim 1, farther comprising:

a buffer memory, coupled commonly with said plurality of nonvolatile semiconductor memories, which holds said first and second sectors of data as write data to be written into said plurality of nonvolatile semiconductor memories,

wherein said control module responds to said write request, carries out read operations of said first and second sectors of data as said write data from said buffer memory and carries out write operations of said first and second sectors of data as said write data read out from said buffer memory into said plurality of nonvolatile semiconductor memories, wherein said write operations into said plurality of nonvolatile semiconductor memories are controlled by sending a first write command from said control module to one of said plurality of nonvolatile semiconductor memories and by sending a second write command from said control module to another of said plurality of nonvolatile semiconductor memories different from said one to which said first write command has been sent while said one of said plurality of nonvolatile semiconductor memories is still performing a write operation responsive to said first write command.

3. A semiconductor storage apparatus according to claim 1, wherein each of said plurality of nonvolatile semiconductor memories is comprised of a flash memory semiconductor chip.

4. A semiconductor storage apparatus according to claim 2, wherein each of said plurality of nonvolatile semiconductor memories is comprised of a flash memory semiconductor chip.

5. A semiconductor storage apparatus according to claim 2, wherein said buffer memory has a storage memory capacity corresponding to a plurality of sectors in units of 512 bytes which is a sector capacity of a standard disk.

6. A semiconductor storage apparatus according to claim 1, wherein said control module includes a processor.

7. A semiconductor storage apparatus according to claim 2, wherein said control module includes a processor

8. A semiconductor storage apparatus according to claim 1, wherein said control module further includes an address controller.

9. A semiconductor storage apparatus according to claim 2, wherein said control module further includes an address controller,

10. A semiconductor storage apparatus according to claim 1, wherein each of said plurality of nonvolatile semiconductor memories is comprised of a flash memory semiconductor chip, and wherein said buffer memory has a storage memory capacity corresponding to a plurality of sectors in units of 512 bytes which is a sector capacity of a standard disk.

11. A semiconductor storage apparatus according to claim 2,

wherein each of said plurality of nonvolatile semiconductor memories is comprised of a flash memory semiconductor chip, and

wherein said buffer memory has a storage memory capacity corresponding to a plurality of sectors in units of 512 byte which is a sector capacity of a standard disk.

12. A semiconductor storage apparatus according to claim 10, wherein said control module includes a processor.

13. A semiconductor storage apparatus according to claim 11, wherein said control module includes a processor.

14. A semiconductor storage apparatus according to claim 10, wherein said control module further includes an address controller.

15. A semiconductor storage apparatus according to claim 11, wherein said control module further includes an address controller.

16. A semiconductor storage apparatus to be coupled with a system bus comprising:

a plurality of nonvolatile semiconductor memories which write data from said system therein in sector units and erase said data in block units, said each block including a plurality of said sectors; and

a control module to be coupled with said system bus, and coupled with said plurality of nonvolatile semiconductor memories,

wherein said control module sends a first erase command to one of said plurality of nonvolatile semiconductor memories to initiate a first internal erase

operation of data in said block units within said one of said plurality of nonvolatile semiconductor memories, and

wherein, after said first erase command has been sent, said control module sends a second erase command to an other of said plurality of nonvolatile semiconductor memories, different from said one of said plurality of nonvolatile semiconductor memories to which said first erase command was sent, to initiate a second internal erase operation of data in said block units within said other of said plurality of nonvolatile semiconductor memories while said one of said plurality of nonvolatile semiconductor memories is still performing said first internal erase operation responsive to said first erase command.

17. A semiconductor storage apparatus according to claim 16, wherein said control module carries out a status polling operation in an order of said nonvolatile semiconductor memories to which said control module sent said erase commands, after said control module sent said erase commands to all of said nonvolatile semiconductor memories.

EVIDENCE APPENDIX

None.

RELATED PROCEEDINGS APPENDIX

None.